Notice of Allowability	Application No.	Applicant(s)	
	09/411,418	CAREY, JOHN A.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/21/05*.

2. ☒ The allowed claim(s) is/are *1-20 and 25-29*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Terminal Disclaimer 10/21/05*.

DETAILED ACTION

1. Claims 1-25 were originally examined.

2. Claims 21-24 are cancelled.

3. Claims 26-29 were added.

Section I: Allowable Subject Matter

4. Claims 1-20,25-29 were examined and allowed.

The following is an examiner's statement of reasons for allowance:

While Warren (US Patent 5,978,870) teaches a computer implemented method for designing an initiator in an integrated circuit, said initiator being connected to an interconnected and arranged to issue packet-format request, said method comprising the steps of (claim 1); a computer implemented method for designing a target in an integrated circuit, said target being connected to an interconnect and arranged to generate packet format response to packet format request, the method comprising the steps of: (claim 3); a computer implemented method for designing an interconnect having routing resources, said interconnect arranged to allow initiators to send packet-format requests to targets, said method comprising the steps of defining: the number of routing resources between the initiator and the target (claim 5); a computer implemented method for designing an interconnect having routing resources, said interconnect arranged to allow targets to send packet-format response to initiators in response to packet-format request from initiators, said method comprising the steps of defining (claim 7); description of an integrated circuit (claims 9-12); a model of an

initiator implemented in a computer to be used in designing an integrated circuit (claim 13); a computer implemented model of a target to be used in designing an integrated circuit (claim 17); a computer implemented method for designing an initiator in an integrated circuit, said initiator being connected to an interconnect and arranged to issue packet-format request, said method comprising the steps of: defining whether the initiator or the interconnect is to be responsible for ordering packet-format responses to requests issued by said initiator (claim 25); none of these references, taken either alone or in combination, with the prior art of record disclose arbiters, including:

(claims 1 and 3) "defining whether the initiator or the interconnect is to be responsible for ordering packet-format responses to packet-format requests issued by said initiator; determining whether to define a maximum number of packet format requests which are permitted to be outstanding at the same time; defining whether a delay stage is required in said initiator; and processing results of the defining steps and the determining step to produce a description of the integrated circuit"

(claim 5)" the arbitration method for arbitration between request; and the association between the routing resources and the targets; and processing results of the defining steps and the determining step to produce a description of an integrated circuit comprising the interconnect"

(claim 7)" the number of routing resources between the target and the initiator; the arbitration method for arbitration between response; the association between the routing resources and the initiator; and producing a description of the integrated circuit based on parameters generated in the defining steps and the determining step"

(claims 9-12) "a computer implemented method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said initiators and said interconnect, said method comprising the steps of: using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled, and selecting one of the plurality of arbitration methods available in said model"

(claim 13) "arranged to send packet request to one or more targets via an interconnect, said model embodied as a plurality of parameters stored in a computer file, said model comprising: an address decode stage running on the computer for identifying the target for which a given message is intended; and a dependency stage running on the computer for determining the allowability of a request, the operation of said dependency stage being selectable, said dependency stage being such that the model supports an arrangement where the initiator or the interconnect is responsible for maintaining the order of packet-format responses from a target to the requests"

(claim 17) "in which one or more initiators are arranged to send packet-format request to a target and the target is arranged to send packet-format responses to the requests via an interconnect, said model embodied as a plurality of parameters stored in a computer file, said model comprising: a locking stage for causing a computer to permit locked transactions to occur if required; and a decode state for causing the computer to decode information stored in a first queue into an address for the response"

(claim 25) " defining whether a delay stage is required in said initiator; storing parameters in a computer file indicating results of the defining steps; and processing the stored parameters to produce a description of the integrated circuit"

While Warren, taken either alone or in combination with the prior art of record discloses arbiters within an integrated circuit, including: producing a description of the integrated circuit, in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Examiner's Amendment

5. An examiner's amendment to the record appears below. Should changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CRF 1.312 . To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Kent Lembke (Registration # 44,866) on 1/9/06.

The application has been amended as follows:

Specification paragraph 0115, lines 2-3 , phrase "164 to 168.", was replaced with -- 164, 166 and 168. -- -- .

Specification paragraph 0126, line 4, after "algorithm part", –198 -- was inserted.

Specification paragraph 0126, line 6, after "algorithm part", –198 -- was inserted.

Section II: Response to Previous Office Action

101/Statutory Double Patenting

6. Applicants are thanked for addressing this issue. Both rejections are withdrawn in view of applicant's amendments to claims and the terminal disclaimer.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Leo Picard ((571) 272-3749). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

December 29, 2005

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

TS